

Claim 1

The Examiner seems to have missed one of the elements of claim 1 that applicant believes makes this claim patentable over the prior art. Specifically, claim 1 requires "decompressing the compressed test pattern into a decompressed test pattern of bits as the compressed test pattern is being provided."

The "decompressor" of the '898 patent does not decompress bits as the compressed bits are being provided. Instead, a compressed seed value is first loaded and only after the seed value is loaded does decompressing start. This is clearly illustrated in the '898 patent in FIGS. 5 through 7 and 12, together with the corresponding discussion at column 11, line 9 through column 12, line 61. Dr. Rajski, the inventor on the '898 patent, confirmed to Applicant's representative that the teaching of the '898 patent is as follows: First starting with the left side of FIG. 12, part of the LFSR 206 (which is the decompressor) includes a multiplexer shown having one input labeled "SEED" and a second input received from XOR gate 208. Thus, the multiplexer either selects the seed input for first loading a seed or a feedback input used during decompression mode. Both loading of the seed and decompressing cannot occur simultaneously. As can be seen on the right side of FIG. 12, a seed is first loaded as shown under the heading "LOAD SEED" and then after the seed is loaded, decompression occurs as shown under the heading "DECOMPRESSION". (See column 11, lines 9 through 35). Specifically, the '898 patent states that "the decompression commences upon resetting LFSR 206, and shifting 2-bits of the compressed seed (1,1) into LFSR 206." (Column 11, lines 33-35).

Thus, the decompressor in the '898 patent does not decompress the test pattern as the compressed test pattern is being provided, as required by claim 1. Instead, the compressed pattern is provided first through loading of the seed and only after that loading is fully completed does the decompression occur.

FIGS. 5 through 7 of the '898 patent provide further details of how the decompression occurs. First, a seed value is stored in a register file 50 (FIG. 5). The register file 50 together with a shifter 48, multiplexer 52, arithmetic logic unit 54, and accumulator 56 are all part of the decompressor. (Column 12, lines 28-31). FIG. 6 shows at 58, that a seed is first loaded into the register file 50 before decompressing. (Column 12, lines 52 through 61). Then after the seed is fully loaded, the decompression begins in steps 60 and 62. (FIG. 6).

As indicated in claim 1 of the present application, decompressing the compressed test pattern is accomplished as the compressed test pattern is being provided. FIG. 5 of the present application shows the parallel inputs 37 providing the compressed data to the decompressor 36 as decompression occurs.

Thus, claim 1 should be in condition for allowance.

Claims 2-18

Claims 2 through 18 depend from claim 1 and should be in condition for allowance for the reasons stated above.

Claims 19-29

Claims 19 through 29 contain a similar limitation regarding decompressing bits as the compressed test pattern is being provided and should be in condition for allowance for the reasons stated above.

Claims 30 and 31

Claim 30 requires that the decompressor have a plurality of input channels that receive in parallel the bits of the compressed test pattern. FIG. 5 of the present application shows an example at 37 of two parallel inputs being received by the decompressor 36.

In contrast, the '898 patent shows only a serial input into the decompressor for loading the seed. (See FIG. 12, single input labeled "SEED").

Claim 31 depends from claim 30 and should also be in condition for allowance.

Claim 32

Claim 32 requires combining bits stored within the machine with bits received from a compressed test pattern. As can be seen in FIG. 12 of the '898 patent, there is only a single input into the decompressor 206, which is labeled "SEED". As a result, in the '898 patent, bits stored in the machine are over written by new bits, rather than "combined" with bits received from a compressed test pattern as required by claim 32.

Claims 33-38

Claims 33 through 38 include limitations similar to those discussed above and should be in condition for allowance for similar reasons.

Claims 39-47

New claims 39 through 47 are dependent claims and should be in condition for allowance as they are based on now allowable independent claims. Support for these claims is in the application. For example, the intermediate register of claim 41 is shown in FIG. 11. No new matter has been added.

CONCLUSION

For the reasons stated above, it is believed that the application is in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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